

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of the Claims:

1 Claim 1. (Currently Amended) An image sensor comprising:

2 a plurality of pixels each having an output, each pixel including:

3 a first circuit that produces a signal proportional to incident
4 light intensity, said first circuit being connected to supply said
5 proportional signal to said pixel output,

6 a select node connected to receive a select signal for selecting
7 said pixel from said plurality of pixels, and

8 a reset transistor for resetting said pixel;

9 an amplifier having:

10 a first input for receiving said outputs of said pixels, and

11 an output connected to said pixels to be actively coupled to said
12 reset transistors during a pixel reset phase to provide a negative
13 feedback signal to a selected pixel during said pixel reset phase; and

14 a reset reference voltage source connected to apply a reset reference voltage
15 signal to said amplifier to provide a voltage reference for controlling reset of said
16 pixels.

1 Claim 2. (Previously Presented) The image sensor of claim 1 wherein said
2 amplifier further includes a second input receiving said reset reference voltage
3 signal.

1 Claim 3. (Previously Presented) The image sensor of claim 2 wherein said
2 reset transistor includes a gate and first and second terminals, said first terminal
3 connected to receive said negative feedback signal to adjust said second terminal's
4 voltage to a selected reset voltage.

1 Claim 4. (Previously Presented) The image sensor of claim 3 wherein said
2 reset reference voltage source signal is selected to control said voltage at said second
3 reset transistor terminal to be about $V_T - \Delta V$ below a reset voltage applied at said
4 gate terminal of said reset transistor, where V_T is a threshold voltage that is
5 characteristic of said reset transistor, and ΔV is selected to maintain said reset
6 transistor in a subthreshold region of operation during a steady state phase of pixel
7 reset.

1 Claim 5. (Previously Presented) The image sensor of claim 4 wherein said
2 selected ΔV is greater than about one hundred millivolts.

1 Claim 6. (Previously Presented) The image sensor of claim 4 wherein said
2 select node of each said pixel comprises a terminal of a row select transistor that is
3 coupled to said first input of said amplifier.

1 Claim 7. (Previously Presented) The image sensor of claim 6 wherein each
2 said pixel further comprises a source follower transistor coupled between said
3 second terminal of said reset transistor and a terminal of said row select transistor.

1 Claim 8. (Previously Presented) The image sensor of claim 3 wherein said
2 first circuit comprises a photocircuit.

1 Claim 9. (Previously Presented) The image sensor of claim 8 wherein said
2 amplifier comprises a differential amplifier including a first differential amplifier
3 input transistor connected to receive said first amplifier input and a second
4 differential amplifier input transistor connected to receive said second amplifier
5 input, said first and second differential amplifier input transistors connected to
6 provide a signal to a current mirror circuit that is connected to deliver said negative
7 feedback signal to said reset transistor first terminal.

1 Claim 10. (Previously Presented) The image sensor of claim 8 wherein said
2 photocircuit includes a photodiode and a capacitance.

1 Claim 11. (Previously Presented) The image sensor of claim 7 wherein said
2 first circuit is a photocircuit.

1 Claim 12. (Previously Presented) The image sensor of claim 11 wherein said
2 photocircuit includes a photodiode and a capacitance.

1 Claim 13. (Currently Amended) An image sensor array having rows and
2 columns of pixels, comprising:

3 at least one column line;

4 a plurality of pixels each having an output, the outputs of pixels in a column
5 being connected to a common respective column line, each said pixel including:

6 a first circuit that produces a signal proportional to incident
7 light intensity, said first circuit being connected to supply said
8 proportional signal to said pixel output, and

9 a reset transistor for resetting said pixel;

10 at least one amplifier, each said amplifier having a first input coupled to at
11 least one said column line, each said amplifier being connected to provide a negative

12 feedback signal to each said pixel reset transistor of a respective column of pixels
13 during each corresponding pixel reset phase; and

14 a reset reference voltage source connected to apply a reset reference voltage
15 signal to each said amplifier to provide a voltage reference for controlling reset of
16 said pixels.

1 Claim 14. (Previously Presented) The image sensor of claim 13 wherein said
2 amplifier further includes a second input for receiving said reset reference voltage
3 signal.

1 Claim 15. (Previously Presented) The image sensor of claim 14 wherein said
2 reset transistor includes a gate and first and second terminals, said first terminal
3 connected to receive said negative feedback signal to adjust said second terminal's
4 voltage to a selected reset voltage.

1 Claim 16. (Previously Presented) The image sensor of claim 15 wherein said
2 reset reference voltage source signal is selected to control said voltage at said second
3 reset transistor terminal to be about $V_T - \Delta V$ below a reset voltage applied at said
4 gate terminal of said reset transistor, where V_T is a threshold voltage that is
5 characteristic of said reset transistor, and ΔV is selected to maintain said reset
6 transistor in a subthreshold region of operation during a steady state phase of pixel
7 reset.

1 Claim 17. (Previously Presented) The image sensor array of claim 16
2 wherein said selected ΔV is greater than about one hundred millivolts.

1 Claim 18. (Previously Presented) The image sensor array of claim 16
2 wherein each pixel comprises a row select transistor coupled between said second
3 terminal of said reset transistor and said first input of said amplifier.

1 Claim 19. (Previously Presented) The image sensor array of claim 18
2 wherein each pixel further comprises a source follower transistor coupled between
3 said second terminal of said reset transistor and a terminal of said row select
4 transistor.

1 Claim 20. (Previously Presented) The image sensor array of claim 16
2 wherein said first circuit of each pixel comprises a photocircuit.

1 Claim 21. (Previously Presented) The image sensor array of claim 20
2 wherein said amplifier comprises a differential amplifier including a first
3 differential amplifier input transistor connected to receive said first amplifier input
4 and a second differential amplifier input transistor connected to receive said second
5 amplifier input, said first and second differential amplifier input transistors
6 connected to provide a signal to a current mirror circuit that is connected to deliver
7 said negative feedback signal to said reset transistor first terminal.

1 Claim 22. (Previously Presented) The image sensor array of claim 20
2 wherein said photocircuit of each active pixel comprises a photodiode and a
3 capacitance.

1 Claim 23. (Previously Presented) The image sensor array of claim 19
2 wherein each said first circuit comprises a photocircuit.

1 Claim 24. (Previously Presented) The image sensor array of claim 23
2 wherein each said photocircuit comprises a photodiode and a capacitance.

1 Claim 25. (Previously Presented) An image sensor array having rows and
2 columns of pixels, comprising:

3 at least one row line;

4 a plurality of pixels each having an output, the outputs of pixels in a row
5 being connected to a common respective row line, each said pixel including:

6 a first circuit that produces a current proportional to incident
7 light intensity, said first circuit being connected to supply said
8 proportional current to said pixel output, and

9 a reset transistor for resetting said pixel;

10 at least one amplifier, each said amplifier having a first input coupled to at
11 least one said row line, each said amplifier being connected to provide a negative
12 feedback signal to each said pixel reset transistor of a respective row ~~if~~ of pixels
13 during each corresponding pixel reset phase; and

14 a reset reference voltage source connected to apply a reset reference voltage
15 signal to each said amplifier to provide a voltage reference for controlling reset of
16 said pixels.

1 Claim 26. (Previously Presented) The image sensor of claim 25 wherein said
2 amplifier further includes a second input for receiving said reset reference voltage
3 signal.

1 Claim 27. (Previously Presented) The image sensor of claim 26 wherein said
2 reset transistor includes a gate and first and second terminals, said first terminal
3 connected to receive said negative feedback signal to adjust said second terminal's
4 voltage to a selected reset voltage.

1 Claim 28. (Previously Presented) The CMOS image sensor of claim 27
2 wherein said reset reference voltage source signal is selected to control said voltage
3 at said second terminal to be about $V_T - \Delta V$ below a reset voltage applied at said gate
4 terminal of said reset transistor, where V_T is a threshold voltage that is
5 characteristic of said reset transistor, and ΔV is selected to maintain said reset
6 transistor in a subthreshold region of operation during a steady state phase of pixel
7 reset.

1 Claim 29. (Previously Presented) The image sensor array of claim 28
2 wherein said selected ΔV is greater than about one hundred millivolts.

1 Claim 30. (Previously Presented) The image sensor array of claim 28
2 wherein each pixel comprises a column select transistor coupled between said
3 second terminal of said reset transistor and said first input of said amplifier.

1 Claim 31. (Previously Presented) The image sensor array of claim 30
2 wherein each pixel further comprises a source follower transistor coupled between
3 said second terminal of said reset transistor and a terminal of said column select
4 transistor.

1 Claim 32. (Previously Presented) The image sensor array of claim 28
2 wherein said first circuit of each pixel comprises a photocircuit.

1 Claim 33. (Previously Presented) The image sensor array of claim 32
2 wherein said amplifier comprises a differential amplifier including a first
3 differential amplifier input transistor connected to receive said first amplifier input
4 and a second differential amplifier input transistor connected to receive said second

5 amplifier input, said first and second differential amplifier input transistors
6 connected to provide a signal to a current mirror circuit that is connected to deliver
7 said negative feedback signal to said reset transistor first terminal.

1 Claim 34. (Previously Presented) The image sensor array of claim 32
2 wherein said photocircuit of each pixel comprises a photodiode and a capacitance.

1 Claim 35. (Previously Presented) The image sensor array of claim 31
2 wherein each said first circuit comprises a photocircuit.

1 Claim 36. (Previously Presented) The image sensor array of claim 35
2 wherein each said photocircuit comprises a photodiode and a capacitance.

1 Claim 37. (Previously Presented) The image sensor of claim 1 wherein said
2 image sensor comprises a CMOS-compatible image sensor.

1 Claim 38. (Previously Presented) The image sensor array of either of claims
2 13 or 25 wherein said image sensor array comprises a CMOS-compatible image
3 sensor array.

1 Claim 39. (Previously Presented) The image sensor of claim 1 wherein said
2 pixels comprise active pixels.

1 Claim 40. (Previously Presented) The image sensor array or either of claims
2 13 or 25 wherein said pixels comprise active pixels.